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(54) **SOLID-STATE IMAGE PICKUP DEVICE**

(57)Abstract:
PROBLEM TO BE SOLVED: To solve a problem of a conventional solid-state image pickup devicewhose pixel is configured with one photodiode4 transistors(TRs) and one capacitorthat cannot have utilized only either of a field shutter function and a kTC (k is Boltzman's constantT is absolute temperature and C is a capacitance) noise cancel function.
SOLUTION: After resetting a capacitor Ce by a TR M1a charge transfer TR M5 is conductive to transfer charges obtained by photoelectric conversion at a photo diode PD to the capacitor Cewhere the charges are stored. Then each TR M5 is turned off simultaneously for all the pixels and Trs M1M3 of pixels on the same row are conductiveto provide a prescribed level to a CDS(correlation dual sampling) circuit 5. Succeedinglya TR M6 is conductive and the TR M3 is turned on to output a signal corresponding to the chargesby a field shutter function stored in the capacitor Ce to the CDS circuit 5. Thusthe CDS circuit transfer can cancel kTC noise.

CLAIMS

[Claim(s)]
[Claim 1]A photo-diode and a converter which transforms into an electrical change an electric charge acquired by said photo-diode carrying out photoelectric conversionA pixel provided with a transistor for reset for resetting

said converter and an output means which outputs potential of said converter to the exteriorMultiple arrays are carried out to two-dimensional matrix form or one-dimensional line formand two in a state of only background noise where a signal level and a signal level from said pixel have not ridden are sampledIn a solid state camera provided with a noise canceller from which a noise is removed by taking the differenceA capacitor for accumulating an electric charge between said photo-diode and said converter into said pixel temporarily is formedBetween said capacitor and said photo-diodethe 1st transistor for charge transferAfter providing the 2nd transistor for charge transfer between said capacitor and said converterrespectivelyoutputting potential of only background noise on which a signal has not ridden by said output means after reset of said converter with said transistor for reset and saving at said noise cancellerCarry out photoelectric conversion with said photo-diodeand an electric charge which was transmitted to all the pixel coincidence and accumulated in said capacitor through said 1st transistor for charge transfer at it is transmitted to said converter through said 2nd transistor for charge transferThe new potential produced in this converter as a result is outputted to said noise canceller by said output meansA solid state camera taking difference with potential of only said background noise beforehand saved in this noise cancellerand having a control means which takes out the difference as a true signal.

[Claim 2]A photo-diode and a converter which transforms into an electrical change an electric charge acquired by said photo-diode carrying out photoelectric conversionA pixel provided with a transistor for reset for resetting said converter and an output means which outputs potential of said converter to the exteriorMultiple arrays are carried out to two-dimensional matrix form or one-dimensional line formand two in a state of only background noise where a signal level and a signal level from said pixel have not ridden are sampledIn a solid state camera provided with a noise canceller from which a noise is removed by taking the differenceThe 1st transistor for charge transfer connected to said photo-diode into said pixelIt is approached and provided between the 2nd transistor for charge transfer connected to said converterand the said 1st and 2nd transistors for charge transferAfter outputting potential of only background noise on which a signal has not ridden after providing a MOS gate which accumulates an electric charge from said photo-diode

directly under it and resetting said converter with said transistor for reset by said output means and saving at said noise cancellerCarry out photoelectric conversion with said photo-diodeand an electric charge which was transmitted directly under said MOS gate and accumulated in all the pixel coincidence through said 1st transistor for charge transfer is transmitted to said converter through said 2nd transistor for charge transferThe new potential produced in this converter as a result is outputted to said noise canceller by said output meansA solid state camera taking difference with potential of only said background noise beforehand saved in this noise cancellerand having a control means which takes out the difference as a true signal.
[Claim 3]The solid state camera according to claim 1 or 2 connecting the 2nd transistor for reset that is switched to a node of said photo-diode and said 1st transistor for charge transfer to arbitrary timingand resets said photo-diode at the time of one.[Claim 4]A photo-diode and the 1st transistor for reset connected to said photo-diodeA converter which transforms into an electrical change an electric charge acquired by said photo-diode carrying out photoelectric conversionThe 2nd transistor for reset for resetting said converterThe multiple arrays of the pixel provided with an output means which outputs potential of said converter to the exterior are carried out to two-dimensional matrix form or one-dimensional line formTwo in a state of only background noise where a signal level and a signal level from said pixel have not ridden are sampledThe 1st transistor for charge transfer that is the solid state camera provided with a noise canceller from which a noise is removed by taking the differenceand was connected to said photo-diode and the 1st transistor for reset into said pixelIt is approached and provided between the 2nd transistor for charge transfer connected to said converterand the said 1st and 2nd transistors for charge transfersaid 1st transistor for reset being set to OFFandafter providing a MOS gate which accumulates an electric charge from said photo-diode directly under it and resetting said photo-diode with said 1st transistor for resetSaid 1st transistor for charge transfer is considered as one in the state where the 1st voltage for setting potential [directly under] of said MOS gate as a middle level at the time of the maximum and the minimum is impressed to said MOS gateSince an electric charge by which photoelectric conversion was carried out is transmitted directly under said MOS gate and stored up with the 1st

shutter time and said photo-diodesaid 1st transistor for charge transfer is made offAfter resetting said photo-diode with said 1st transistor for reset againSaid 1st transistor for charge transfer is considered as one in the state where the 2nd voltage for making said 1st transistor for reset offand setting potential [directly under] of said MOS gate as a larger level than said 1st voltage is impressed to said MOS gateA solid state camera having a control means which makes off said 1st transistor for charge transfer since an electric charge by which photoelectric conversion was carried out is transmitted directly under said MOS gate and stored up with the 2nd shutter time shorter than said 1st shutter time and said photo-diode.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the CMOS image sensor which was applied to the solid state cameraespecially had a store-and-forward part in the pixel.
[0002]
[Description of the Prior Art]It roughly divides into the conventional solid state cameraand there are twoa CCD system and a CMOS sensor systemin it. The difference among both is in the place referred to as how to give the information on the electric charge of the photo-diode instead of the photo-diode which changes light into an electric charge out of each photo detector.
[0003]A CCD system transmits directly the electric charge generated in the photo-diode to the exterior by a charge coupled device (CCD:charge coupled device). On the other handa CMOS sensor system is outputted to the element exterior through the amplifier in which the information on the potential by the electric charge generated in the photo-diode was provided corresponding to each photo-diode. Since the pixel structure of this CMOS sensor system can be created in the almost same process as the usual CMOS-LSI processthe line for CMOS-LSI can be used as it isand there is a merit that an area sensor and other CMOS circuits can be intermingled.
[0004]On the other handthere is a problem that fixed pattern noise is loud compared with a CCD system in a CMOS sensor system. Fixed pattern noise mainly originates in the variation in the threshold voltage of the transistor for amplifier.

[0005]Drawing 7 shows the block diagram of an example of the conventional solid state camera.This conventional solid state camera shows the most common CMOS image sensor. Pixel 2_{11}-2_{33} etc. are arranged at two-dimensional matrix formand with the vertical shift register 1 among these pixel 2_{11} - 2_{33}. Operation of two or more (arranged horizontally) pixels of each line is controlled for every line (it usually goes to a lower line from the upper line)and the signal from each pixel 2_{11}-2_{33}It is inputted into load and the noise canceller 3and after noise cancellation operation is carried outone by one with the horizontal shift register 4and the signal of each sequence is outputted as an imaging signal. [the transistor T1 - T3]
Usuallyprocessing follows processing to a left sequence from a right sequence. A row and column can also be arranged conversely. It is also possible to arrange a pixel not to two-dimensional matrix form but to the one-dimensional line form of one row.
[0006]The noise canceller called a CDS circuit with a pixel is attached to the solid state camera of this formeri.e.the conventional CMOS image sensor. There is this in order to remove background noise (mainly variation of the threshold voltage of the transistor for amplifier of a pixel) when the signal is not contained from the output signal of a pixel.
[0007]Drawing 8 shows the representative circuit schematic of an example for 1 pixel of the conventional solid state camera called a CMOS image sensor.Identical codes are given to drawing 7 and an identical configuration portion among the figure.The one pixel 2a consists of one photo-diode PDthe transistors M1 for reset by which the source was connected to the N type layer of photo-diode PDthe transistors M2 for amplification by which the gate was connected to the N type layer of photo-diode PDand the transistors M3 for transmission in drawing 8. The transistor M1M2and M3 are MOS type field effect transistors (FET)and are usually FET of an n channel.
[0008]The source of the transistor M2 is connected to the double correlation sampling (CDS) circuit 5 and the load 6 through the transistor M3 with a switch function.
The transistor M3 operates as a source follower circuit.
CDS circuit 5 comprises the two capacitors C1 and C2 and the two switches S1 and S2.
The non-grounded side terminal of the capacitor C1 is connected to the source of the transistor M3 via the switch S1 and the capacitor C2 in seriesThe switch S1 side

terminal C2a of the capacitor C2 is connected to the reference voltage Vref via the switch S2and the switch S1 side terminal C1b of the capacitor C1 is connected to the signal output line via the switch S3.

[0009]CDS circuit 5 and the load 6 are the circuitry portions for one row of pixels the load of drawing 7and among the noise cancellers 3. CDS circuit 5 samples two in the state of only background noise where the signal level and signal level from a pixel have not riddenand carries out the role of the noise canceller from which a noise is removed by taking the difference. A current regulator circuit is usually used for the load 6.

[0010]Nextoperation of equipment is explained conventionally [this].Nowthe pixel 2a in drawing 8 presupposes that it is a pixel of a sequence with the line of somewhere middle which are not the top line and a lowermost row. Firstthe transistor M1 is made off [one and the transistor M3]and makes a reset state the terminal T1 by the side of the N type layer of photo-diode PD. Potential of the terminal T1 at this time is made into reset voltage (Vdd-Vthrst). HereVdd is power supply voltage and Vthrst is the threshold voltage of the transistor M1. At this reset statesince the transistor M3 is offthere is no output from this pixel 2a in a column signal line.

[0011]Nextthe light from a photographic subject is entered into photo-diode PDand photoelectric conversion is made to performwhere the transistor M1 is made off. Therebythe electric charge according to incident light quantity is accumulated in photo-diode PD. The capacity Cpxl in the terminal T1 serves as the capacity Cpd of photo-diode PDand gate capacitance Camp of the transistor M2 from the diffusion capacitance Crst of the transistor M1and the stray capacitance Cf of wiring. If the amount Q of net charge occurs in photo-diode PDthe electrical change of only **V=Q/Cpxl will occur in this terminal T1. On the other handCDS circuit 5 is processing the output signal of the pixel of other lines in the meantime.

[0012]Processing of the output signal of the pixel (not shown) of the continued line of the pixel 2a which CDS circuit 5 is observing is endedand if a processing result is outputted through the switch S3 closed with the horizontal shift register 4CDS circuit 5 will start processing of the pixel 2a currently observed. CDS circuit 5 performs its reset action first.

[0013]That isthe switch S1 and S2 are closed and potential of the terminal C2a and the terminal C1b is set to reference-potentials Vref. If high-level voltage is

impressed to the gate of the transistor M3 in this state and M3 is made oneThe potential (Vdd-Vthrst+**V) of the terminal T1 of photo-diode PD is amplified with the transistor M2and also the potential which lets the drain of the transistor M3 and a source pass (Vdd-Vthrst-Vthamp+**V) is outputted to a column signal line (that isterminal C2b). Therebythe potential difference of (Vdd-Vthrst-Vthamp+**V-Vref) is built over the capacitor C2. HereVthamp is the threshold voltage of the transistor M2.

[0014]Thenthe switch S2 is openedreset voltage is impressed to the gate of the transistor M1and M1 is considered as one. Thensince the potential of the terminal T1 of photo-diode PD serves as (Vdd-Vthrst)the potential of terminal C2b serves as (Vdd-Vthrst-Vthamp). It means thatas for terminal C2bpotential had changed by this only in (Vdd-Vthrst-Vthamp)-(Vdd-Vthrst-Vthamp+**V) =-** V. This is equal to a part for the voltage change by the side of the terminal T1 of photo-diode PD. Thereforeonly the amount of [by the photoelectric conversion of photo-diode PD] voltage change is able to take out purely by a series of above-mentioned operations.

[0015]As a resultas for the potential of the terminal C2a (= terminal C1b)only the proportional component with which the capacitor C1 and C2 were connected in series by voltage change part **V changes. That isVref-{**V-C1/(C1+C2)} (1) It becomes. Thenthe switch S1 is opened and it supposes that it is offand a processing result is held to the capacitor C1and it stands by to it. Thenthe transistor M3 is come by off and that of the output from the pixel 2a is lost.Thenthe processing result of (1) type which the switch S3 was closed to a certain timingand was held with the horizontal shift register 4 of drawing 7 at the capacitor C1 is outputted as a pixel signal. Thenthe switch S3 opensit is supposed that it is offand it returns to the first reset state. The operation same also about each pixel as the above is performed.[0016]Howeverin the CMOS image sensor of drawing 8shutter functions pose a problem. That isin CCDsince carriers are moved from a photo-diode to a transfer region all at once at a certain momentthe picture information obtained from CCD has simultaneity in all the pixels in 1 screenand CCD has shutter functions intrinsically.

[0017]On the other handsince the CMOS image sensor of drawing 8 is read in order for every linethe picture created using this information shows time to be different for every line. Thereforeit will be the perverted picture if Still Picture Sub-Division is taken out. The shutter of

such picture shifted in time is called rolling shutter in many cases.
[0018]The shutter which makes Still Picture Sub-Division to which it was equal in time on the other hand is called field shutter in many cases. One method of giving a field shutter function with the conventional CMOS image sensor of the composition of drawing 8 only with the function of a rolling shutter is providing a mechanical shutter. That isa mechanical shutter is provided in addition to an elementand only a certain specific time should open a shutter. Howeverin this methodcost becomes high and photography of an animation is difficult.
[0019]In order to attach a field shutter functionit is indispensable to have a switch which takes out a certain instantaneous picture information simultaneously by all the pixelsand an accumulating part which stores it temporarily. Thenthe transistor M4 and the capacity Ce are usually applied to a picture element part like drawing 9and it realizes. Identical codes are given to drawing 8 and an identical configuration portion among the figureand the explanation is omitted.In drawing 9with MOS transistor M4 by which the drain and the source were further connected to the pixel 2a of drawing 8 between the N type layer of photo-diode PDand the terminal T1one end is connected to the terminal T1and pixel 2b has the feature in the point of having added further the capacitor Ce for adjustment by which the other end was grounded. The transistor M4 takes charge of shutter functionsand the capacitor Ce takes charge of an accumulating function. The gate capacitance of the transistor M2etc. may be enough as the capacitor Ceand it does not need to form the capacitor Ce in particular in that case. The operation at the time of having such composition is shown below.
[0020]Pixel 2b presupposes that it is a pixel of a sequence with the line of somewhere middle which are not the top line of a picture element partand a lowermost row. In explaining the cycle of operation of a pixelit carries out [that the output of the information last now just finished and].The transistor M1M3and M4 are come by off in this state. The potential of the terminal T1 at this time is (Vdd-Vthrst). HereVdd is power supply voltage and Vthrst is the threshold voltage of the transistor M1. Since the terminal T1 was not connected anywhere but has floated electrically at this timeit is still reset potential. Since the transistor M3 is offthere is no output from pixel 2b in a column signal line. Photoelectric conversion is performed in photo-diode PD which the transistor M4 also serves as

OFFtherefore is electrically separated from the terminal T1 on the other hand.Performing photoelectric conversion in this wayit is waiting for pixel 2b until the information on the pixel of all the lines below itself is read.[0021]In this wayone [the transistors M4 of all the pixels] all at once if the signal of all the pixels is read and predetermined time passes after a photoelectric conversion start. Thenthe electric charge accumulated in the N type layer side of photo-diode PD is simultaneously transmitted to the terminal T1 by all the pixels. As a resultthe electric charge of photo-diode PD is lost and PD is reset. After transmission is completedthe transistor M4 is come by off and photo-diode PD starts photoelectric conversion again.

[0022]The capacity Cpxl of the terminal T1 consists of the capacitor Cegate capacitance Camp of the transistor M2and the diffusion capacitance Crst of the transistor M1 and the stray capacitance Cf of wiring. Thereforeif the transmitted amount of net charge sets to Qthe electrical change of only **V=Q/Cpxl will happen to the terminal T1. Since the carrier transmitted is an electronthe electric charge Q is a negative valuetherefore **V is also a negative value. Since the potential of the terminal T1 was (Vdd-Vthrst) before charge transferafter charge transfer is set to (Vdd-Vthrst+**V).

[0023]After transmission of an electric charge is completed by all the pixelsCDS circuit 5 performs signal processing for every line. While processing other linespixel 2b currently observed stands by holding an electric charge to the capacitor Ce connected to the terminal T1. And CDS circuit 5 starts processing of pixel 2b currently observed. Firstits reset action is performed. That isas mentioned abovethe switch S1 and S2 are closed and potential of the terminal C2a and the terminal C1b is set to reference-potentials Vref. At this timethe switch S3 is opened and is come by off. If high-level voltage is impressed to the gate of the transistor M3 in this state and M3 is made onethe potential of (Vdd-Vthrst-Vthamp+**V) will be outputted to a column signal line (getting it blocked terminal C2b). Therebythe potential difference of (Vdd-Vthrst-Vthamp+**V-Vref) is built over the capacitor C2.

[0024]Thensince it is not anywhere connected with the terminal C2a (= terminal C1b) if the switch S2 is opened and it turns OFFwill be floated electrically. Herethe transistor M1 is once made oneit turns OFF after predetermined timeand the terminal T1 is reset. Thensince the potential of the terminal T1 serves as (Vdd-Vthrst)the

potential of terminal C2b serves as (Vdd-Vthrst-Vthamp). Thereforeit means thatas for the potential of terminal C2bonly (Vdd-Vthrst-Vthamp)-(Vdd-Vthrst-Vthamp+**V) =-** V had changed. This is an ingredient proportional to the charge quantity Q generated in photo-diode PD. Thereforeonly the amount of [by the photoelectric conversion of photo-diode PD] signal is able to take out purely by a series of above-mentioned operations.
[0025]As a resultas for the potential of the terminal C2a (= terminal C1b)only the proportional component with which the capacitor C1 and C2 were connected in series by change part-**V changes. That isonly the same value as the aforementioned (1) formula changes. Thenthe switch S1 is opened and it supposes that it is offand a processing result is held to the capacitor C1and it stands by to it. Thenthe transistor M3 is come by off and that of the output from pixel 2b is lost.Thenthe processing result of (1) type which the switch S3 was closed to a certain timingand was held with the horizontal shift register 4 of drawing 7 at the capacitor C1 is outputted as a pixel signal. Thenthe switch S3 opensit is supposed that it is offand it returns to the first state. In this wayone cycle of a series of processings is completedand the same operation as the following is repeated.[0026]
[Problem to be solved by the invention]Howevera serious problem is among the CMOS image sensors with a field shutter function which are the conventional solid state cameras shown in above-mentioned drawing 9. That isin the conventional equipment of drawing 9after transmitting the electric charge of photo-diode PD to the terminal T1 reset beforehandgenerating potential with it and outputting it out of a pixelit is reset again and used as the level of the standard for cancellation. That isthe reset action of different timing is used in the time of outputting a signaland the time of outputting a background. Thuswhen the voltage by the reset action of another timing is comparedthere is a problem that a kTC noise is not removed.
[0027]This kTC noise is the noise resulting from electronic thermal agitation. For examplemaking potential of a certain capacity C into a certain potential V is giving the electron of the electric charge q to the capacity C only several predeterminedn piece (or it removes) like drawing 10. Several of the n can be expressed like a following formula.
[0028]
n=V/(C-q) (2)
If switch S4 is opened after connecting the capacity C with

the power supply of the voltage V via the resistance R and switch S4closing switch S4 and sufficiently long time's passingas shown in drawing 10 as concrete operationan above-mentioned number of electrons are stored in the capacity Cand both ends have the voltage V.

[0029]Howeversince the electron is carrying out thermal agitation at random actuallywhile having closed switch S4the number of the electron number in the capacity C of electronic increases more than n at a certain timeand there is variation in time as smaller than nwhen another. For this reasonwhen switch S4 is opened and it turns OFFit is more than n in be alike by chanceor there will be few electron numbers which remained in the capacity C then. This variation serves as noise called a kTC noiseand appears. kTC -- k: -- they are a Boltzmann constantT:absolute temperatureand C:capacity -- the noise level Vi -- rms -- Vi=root(kT/C) (3)

It is expressed. (3) As shown in a formulait is the feature to depend for this noise level Vi only on temperature and capacity.

[0030]Thereforein the terminal T1 of a CMOS image sensor of drawing 9if a thing of timing of two different reset is comparedthe noise level Vi1 and Vi2 differentrespectively can remainand cannot cancel. There is no correlation in such noise level Vi1 and Vi2when comparing a thing which is not such correlateda kTC noise is root Doubledand it is Vi'=root (2 kT/C) (4).

It becomes.

[0031]As shown in the above-mentioned (3) types and (4) typesa kTC noise becomes so large that capacity is small. For this reasonwith composition of drawing 8 and drawing 9if a pixel is miniaturizedit will become impossible to take large Cpxl graduallyand a kTC noise will become large.

[0032]Herea kTC noise is estimated quantitatively. For examplesuppose that the capacity Cpxl of the terminal T1 was set to 8fF. A numerical value of these 8fF is a numerical value which is tinged with a touch of realitywhen pixel size becomes below a 5-micrometer mouth. At this timekTC noise part Vi' is set to about 1 mV at a room temperature of T= 300 degrees K. If a noise considers it only as a kTC noise by 2V in the peak magnitude of a signala S/N ratio of the above-mentioned CMOS image sensor with a field shutter function will be set to 46 dB. Since it is said that a S/N ratio of a CCD system is not less than 60 dBit is only a kTC noise and it turns out that performance is considerably inferior as compared with a CCD system.

[0033]In CMOS image sensor composition of the easiest structure of aforementioned drawing 8since the capacity Cpd of photo-diode PD is quite large in capacity of the terminal T1a problem is smaller than a case of composition of drawing 9. Howeverit is impossible to remove a kTC noise with composition of drawing 8.

[0034]Since there are more transistors than composition of drawing 8 when it miniaturizesit becomes impossible on the other handto cleave big capacity gradually for the terminal T1 in the conventional CMOS image sensor of composition of drawing 9. Thereforethe composition of drawing 9 of the necessity of controlling a kTC noise is higher. In composition of this drawing 9if not a field shutter but rolling shutter operation is performeda kTC noise is removable.

[0035]Rolling shutter operation is performed as follows with the composition of drawing 9. Firstthe transistor M4 and M3 presuppose that it is off. At this timethere is no output from this pixel 2b in column signal line C2b. At this timelight enters into photo-diode PD of pixel 2bphotoelectric conversion is performedand an electric charge is accumulated in photo-diode PD. CDS circuit 5 is processing the signal of the element of other lines.

[0036]Nextprocessing of the line currently observed starts. And the terminal T1 is reset by (Vdd-Vthrst). [the transistor M1] Thenthe transistor M1 is turned off.Thenthe transistor M3 is considered as one. At this timethe transistor M4 is still OFF. Therebya signal (Vdd-Vthrst-Vthamp) when the terminal T1 is reset is outputted to a column signal line. In CDS circuit 5the switches S1 and S2 are closedand the potential difference of (Vdd-Vthrst-Vthamp-Vref) is saved to the capacitor C2.

[0037]Nextthe switch S2 is opened and suppose that it is off. Thenthe transistor M4 is considered as one. Therebythe electric charge of photo-diode PD flows into the terminal T1 through the drain of the transistor M4and a source. The capacity Cpxl of the terminal T1 serves as the capacitor Ce and gate capacitance Camp of the transistor M2 from the diffusion capacitance Crst of the transistor M1and the stray capacitance Cf of wiring. If the amount of net charge of photo-diode PD is set to Qthe electrical change of only **V=Q/Cpxl will occur in this terminal T1. The potential of this terminal T1 is amplified with the transistor M2lets the transistor M3 which is one passand is outputted to a column signal line as (Vdd-Vthrst-Vthamp+**V).

[0038]Therebysince change of the potential of terminal C2b is set to (Vdd-Vthrst-Vthamp+**V)-(Vdd-Vthrst-

Vthamp)=+**Vpotential Vref+ {**V-C1/(C1+C2)} proportional to it appears in the terminal C1b. This potential is outputted to the horizontal shift register 4. Thenthe transistor M3 is made off and it is considered as the first reset state.

[0039]Since reset will be performed only once but background noise will be removed from a signal in the same reset action if it does in this waya kTC noise can also be removed. Since there is such the characteristiccomposition like drawing 9 is used in little rolling shutter operation of noise rather than for field shutter operation in many cases.

[0040]Thussince the accumulating function part and the electric charge voltage converting function part were independently the photoelectrical load conversion function part of photo-diode PDand temporarily [electric charge]respectively with neither of the conventional solid state camerasdrawing 8 nor drawing 9In the solid state camera of the pixel configuration set to one photo-diode PD like drawing 8 from the three transistors M1-M3. The three above-mentioned function parts are unitedwhile there is the feature of being constitutionally very simplea field shutter function and a kTC noise cancel function cannot be realized as the resultbut there is a problem that high-definition Still Picture Sub-Division equal in time cannot be obtained.[0041]In the solid state camera of the pixel configuration which consists of one photo-diode PD shown in drawing 9the four transistors M1-M4and the one capacitor Ce. While Still Picture Sub-Division equal in time with a field shutter function can be obtainedthere is a problem that only one of a field shutter function and the kTC noise cancel functions can be used.

[0042]This invention was made in view of the above pointand an object of this invention is to provide the solid state camera which can realize simultaneously a field shutter function and a kTC noise cancel function.

[0043]Other purposes of this invention are to make area of a photo-diode small and to provide the solid state camera of composition advantageous to a miniaturization.

[0044]

[Means for solving problem]The converter which transforms into an electrical change the electric charge acquired by a photo-diode and a photo-diode carrying out photoelectric conversion in order that this invention may attain the above-mentioned purposeA pixel provided with the transistor for reset for resetting a converter and the output means which outputs the potential of a converter to the

exteriorMultiple arrays are carried out to two-dimensional matrix form or one-dimensional line formand two in the state of only background noise where the signal level and signal level from a pixel have not ridden are sampledIn the solid state camera provided with the noise canceller from which a noise is removed by taking the differenceThe capacitor for accumulating an electric charge between a photo-diode and a converter into a pixel temporarily is formedBetween a capacitor and a photo-diodethe 1st transistor for charge transferAfter providing the 2nd transistor for charge transfer between a capacitor and a converterrespectivelyoutputting the potential of only the background noise on which a signal has not ridden by an output means after reset of a converter with the transistor for reset and saving at a noise cancellerCarry out photoelectric conversion with a photo-diodeand the electric charge which was transmitted to all the pixel coincidence and accumulated in the capacitor through the 1st transistor for charge transfer at it is transmitted to a converter through the 2nd transistor for charge transferThe new potential produced in the converter as a result is outputted to a noise canceller by an output meansdifference with the potential of only the background noise beforehand saved in the noise canceller is takenand it has composition which has a control means which takes out the difference as a true signal.
[0045]After accumulating in a capacitor the electric charge acquired by carrying out photoelectric conversion simultaneously with the photo-diode of all the pixels in this inventionAfter making the potential of only the background noise on which it faces outputting to the exterior through an output meansthe transistor for reset and an output means are operatedand a signal has not ridden send out and save to a noise cancellerBy outputting the signal corresponding to the electric charge accumulated in the capacitor to a noise canceller through an output means from a converteronly the signal component proportional to the electric charge produced by the photoelectric conversion of the photo-diode in the noise canceller can be taken out.
[0046]In order to attain the above-mentioned purposethis inventionThe 1st transistor for charge transfer connected to the photo-diode into the pixelIt is approached and provided between the 2nd transistor for charge transfer connected to the converterand the 1st and 2nd transistors for charge transferThe MOS gate which accumulates the electric charge from a photo-diode is provided directly

under itAfter outputting the potential of only the background noise on which a signal has not ridden after resetting a converter with the transistor for reset by an output means and saving at a noise cancellerCarry out photoelectric conversion with a photo-diodeand the electric charge which was transmitted directly under the MOS gate and accumulated in all the pixel coincidence through the 1st transistor for charge transfer is transmitted to a converter through the 2nd transistor for charge transferThe new potential produced in the converter as a result is outputted to a noise canceller by an output meansdifference with the potential of only the background noise beforehand saved in the noise canceller is takenand it has composition which has a control means which takes out the difference as a true signal.

[0047]After accumulating the electric charge acquired by carrying out photoelectric conversion simultaneously with the photo-diode of all the pixels in this invention directly under a MOS gateAfter outputting the potential of only the background noise on which it faces outputting to the exterior through an output meansthe transistor for reset and an output means are operatedand a signal has not ridden by an output means and making it save at a noise cancellerBy outputting the signal corresponding to the electric charge accumulated directly under the MOS gate to a noise canceller through an output means from a converteronly the signal component proportional to the electric charge produced by the photoelectric conversion of the photo-diode in the noise canceller can be taken out.

[0048]Hereit is switched to the node of a photo-diode and the 1st transistor for charge transfer to arbitrary timingand reset of a photo-diode can be performed to arbitrary timing by connecting the 2nd transistor for reset that resets a photo-diode at the time of one.

[0049]In order to attain the above-mentioned purposethis inventionA photo-diode and the 1st transistor for reset connected to the photo-diodeThe converter which transforms into an electrical change the electric charge acquired by a photo-diode carrying out photoelectric conversionA pixel provided with the 2nd transistor for reset for resetting a converter and the output means which outputs the potential of a converter to the exteriorMultiple arrays are carried out to two-dimensional matrix form or one-dimensional line formand two in the state of only background noise where the signal level and signal level from a pixel have not ridden are sampledThe 1st transistor for charge transfer that is the solid state camera provided with the noise canceller

from which a noise is removed by taking the differenceand was connected to a photo-diode and the 1st transistor for reset into the pixelThe 2nd transistor for charge transfer by which the end was connected to the output meansand the 2nd transistor for reset connected to the 2nd transistor for charge transfer and output meansrespectivelyIt is approached and provided between the 1st and 2nd transistors for charge transferand the MOS gate which accumulates the electric charge from a photo-diode directly under it is established in each of each pixelAfter resetting a photo-diode with the 1st transistor for resetIn the state where the 1st voltage for making the 1st transistor for reset offand setting the potential [directly under] of a MOS gate as the middle level at the time of the maximum and the minimum is impressed to a MOS gateconsider the 1st transistor for charge transfer as oneand The 1st shutter timeSince the electric charge by which photoelectric conversion was carried out is transmitted directly under a MOS gate and stored up with a photo-diodethe 1st transistor for charge transfer is made offAfter resetting a photo-diode with the 1st transistor for reset againThe 1st transistor for charge transfer is considered as one in the state where the 2nd voltage for making the 1st transistor for reset offand setting the potential [directly under] of a MOS gate as a larger level than the 1st voltage is impressed to a MOS gateSince the electric charge by which photoelectric conversion was carried out is transmitted directly under a MOS gate and stored up with the 2nd shutter time shorter than the 1st shutter time and a photo-diodeit has composition which has a control means which makes the 1st transistor for charge transfer off.[0050]In this inventionthe electric charge which carried out photoelectric conversion to the electric charge which carried out photoelectric conversion with the photo-diode by the 1st shutter time of the longer one with the photo-diode by the 2nd shutter time of the shorter one can be added directly under a MOS gate.

[0051]

[Mode for carrying out the invention]Nextan embodiment of the invention is described with Drawings. Drawing 1 shows the representative circuit schematic of one pixel circuit of a 1st embodiment of the solid state camera which becomes this invention.Identical codes are given to drawing 8drawing 9and an identical configuration portion among the figure.According to a 1st embodiment shown in drawing 1compared with pixel 2b of drawing 9a MOS type field effect transistor (FET) and one capacitor are addedrespectivelyand

the pixel 2c is made one photo-diodefive transistorsand 2 capacitor composition. Namelyas for the pixel 2cthe N type layer side of photo-diode PD is connected to the source of the transistor M1 for resetand the gate of the transistor M2 in the node (terminal) T1 via the drain of the transistor M5a source and the drain of the transistor M6and the sourcerespectively.[0052]The common node of the transistors M5 and M6 is grounded via the capacitor Cex.The terminal T1 is grounded via the capacitor Ce. The source of the transistor M2 is connected to CDS circuit 5 and the load 6 via the drain of the transistor M3 for an outputand the sourcerespectively.The capacitor Cex consists of N^- diffusion zones made for exampleto p substrate face.In particular when the sum total of gate capacitance Camp of the transistor M2the diffusion capacitance Crst of the transistor M1and the stray capacitance Cf of wiring is enough as the capacity Cpxl of the terminal T1it is not necessary to form the capacitor Ce. The capacity Cpxl of the terminal T1 constitutes the converter which transforms into voltage the electric charge mentioned above with the capacitor Ce.

[0053]Nextoperation of this embodiment is explained.Herethe pixel 2c presupposes that it is a pixel of a sequence with the line of somewhere middle which are not the top line of a picture element partand a lowermost row. Switching control of each transistor M1M3M5and M6 is performed based on the signal from the control circuit which is not illustrated.[0054]It begins from the place said [that the output of the last signal of this pixel 2c has just finished as a starting point of motion cycle explanationand].In this statethe transistor M1 and M6 are off and the terminal T1 is in the state where it floated electrically. In the last cyclephoto-diode PD carried out photoelectric conversion to the terminal T1and the transistor M5 and the electric charge transmitted through M6 remain in it as it is.The transistor M3 also serves as OFF and there is no output from this pixel 2c to a column signal line.

[0055]On the other handthe transistor M5 also serves as OFFand photo-diode PD performs photoelectric conversion in the state where it dissociated from others electricallyand is accumulating the electric charge. The electric charge which suited the capacitor Cex is transmitted to the terminal T1 through the transistor M6and is in the state where there is no electric charge in the capacitor Cex.[0056]In such the statethe pixel 2c is waiting for CDS circuit 5 to end the processing which is a pixel of other

lines. The one [the transistors M5 / all the pixels including the pixel 2c] all at once after signal read-out from all the pixels is completed. Thenthe electric charge Q accumulated in photo-diode PD is simultaneously transmitted to each capacitor Cex through each transistor M5 by all the pixels.As a resultthe electric charge of photo-diode PD is lost and is reset.It is supposed after the end of charge transfer that the transistor M5 is offagainphotoelectric conversion of photo-diode PD is carried outand it starts accumulation of an electric charge.

[0057]Thenthe pixel 2c stands bywhile CDS circuit 5 is carrying out processing which is a pixel of other lines. If processing of the pixel 2c currently observed startsthe pixel 2c will perform the reset action of the terminal T1. That isthe high-level signal from the control circuit which is not illustrated is impressed to the gate electrode of the transistor M1and makes M1 one. At this timethe transistor M3 and M6 are still OFF. As a resultthe potential of the terminal T1 serves as (Vdd-Vthrst). HereVdd is power supply voltage and Vthrst is the threshold voltage of the transistor M1.

[0058]Thenthe signal to the gate electrode of the transistor M1 serves as a low leveland is made off [M1]. Therebythe terminal T1 returns to the state where it floated electricallyand a reset action completes it. Since the kTC noise ingredient Vktc rides on the terminal T1 at this timethe potential of the terminal T1 serves as (Vdd-Vthrst+Vktc). Although Vktc was not specified during explanation of conventional technologyit decides to be shown in order to show clearly that it is removable by this embodiment.[0059]On the other handthe preparations for carrying out signal processing of the pixel 2c even in CDS circuit 5 are made. That isthe switch S1 and S2 are closed and the terminal C2a and C1b are made into the reference potential Vref. Since M3 is considered as one by impressing a high-level signal from the control circuit which is not illustrated to the gate electrode of the transistor M3 in this statethe potential of (Vdd-Vthrst+Vktc-Vthamp) is outputted to multiple-message-transmission item output linei.e.terminalC2b. HereVthamp is the threshold voltage of the transistor M2 for amplification. As a resultthe potential difference of (Vdd-Vthrst+Vktc-Vthamp-Vref) is built over the capacitor C2.

[0060]NextCDS circuit 5 opens the switch S2sets it to OFFand changes the terminal C2a (= terminal C1b) into the state where it floated. Hereit is considered as one by impressing a signal with the transistor M6 high-level from the control

circuit which is not illustrated to the gate electrode.Thenthe electric charge Q currently held at the capacitor Cex is transmitted to the terminal T1 through the transistor M6. The transistor M6 after charge transfer completion is made off. As a resultan electric charge is lost to the capacitor Cex and it will be in the state where it was reset to it.

[0061]On the other handfor the terminal T1the electrical change by the electric charge Q is generated.Although the capacity Cpxl of the terminal T1 consists of the capacity of the capacitor Cegate capacitance Camp of the transistor M2and the diffusion capacitance Crst of the transistor M1 and the stray capacitance Cf of wiringwhen the electric charge Q enters herethe electrical change of **V=Q/Cpxl occurs.Thereforethe potential of the terminal T1 is set to (Vdd-Vthrst+Vktc+**V).

[0062]If an electrical change happens to the terminal T1it will be amplified by the source follower circuit with the transistor M2and also will be told through the transistor M3 in an ON state to multiple-message-transmission item output linei.e.terminalC2b.Therebythe potential of terminal C2b is set to (Vdd-Vthrst+Vktc-Vthamp+**V). That isthe electrical change produced in terminal C2b is (Vdd-Vthrst+Vktc-Vthamp+**V)-(Vdd-Vthrst+Vktc-Vthamp)=**VIt is influenced only by the ingredient by the charge quantity Q by the photoelectric conversion of photo-diode PDbut there is also no influence of a kTC noise.

[0063]According to the electrical change of this terminal C2bthe electrical change of proportionality part Vref+{**V-C1/(C1+C2)} with which the capacitor C1 and C2 were connected in series produces the terminal C2a (= terminal C1b) which is in the state which floated electrically.Thenthe switch S1 is openedit supposes that it is offand the processing result which is the above-mentioned electrical change is held to the capacitor C1. And it is supposed that the transistor M3 is off and the output from the pixel 2c is lost.Thenthe switch S3 is considered as one with the horizontal shift register which is not illustratedand the processing result of the pixel 2c currently held at the capacitor C1 is outputted as a pixel signal through the switch S3.Thenthe switch S3 is opened againit is supposed that it is offand one cycle in this pixel 2c is completed. In the backthe same thing is again repeated from the beginning.[0064]Explanation of operation of the above-mentioned embodiment is an exampleand is not limited to this.For examplewhat is necessary is to perform reset with the transistor M1 of the terminal T1 by the

above-mentioned explanationjust before outputting the reset potential of the terminal T1but just to perform it once to [somewhere in] the next signal output operationafter it is not limited to this and the last signal output finishes.For exampleimmediately after the last signal output finishesthe transistor M1 is made oneand it may be made to perform the reset action of the terminal T1 first of all.
[0065]Although reset of the capacitor Cex is performed by transmitting the stored charge of Cex thoroughly by the above-mentioned explanationit cannot transmitif there is too much stored chargeand the phenomenon in which an electric charge remains in Cex may ariseand it may serve as an afterimage.For this reasonbefore and transmitting an electric charge to the capacitor Cex from photo-diode PDonceand it may be made to perform operation which resets the capacitor Cex compulsorily. [the transistor M5] [the transistors M1 and M6]
[0066]thusthe background noise out of the signal [according to this embodiment] according to the charge transfer of photo-diode PD in CDS circuit 5 -- it is (Vdd-Vthrst-Vthamp+Vktc) -- it being removed andSince voltage change part **V proportional to the amount Q of net charge produced by the photoelectric conversion of photo-diode PD can take out to multiple-message-transmission item output line C2b purelythe cancel function of a kTC noise is realizable.
[0067]It is also possible only for predetermined time to hold an electric charge to the capacitor Cex. Since the electric charge acquired by carrying out photoelectric conversion of the light which entered simultaneously to the photo-diode of all the pixels containing photo-diode PD in this embodiment is transformed into voltage and he is trying to output ita field shutter function can be realized and Still Picture Sub-Division in the same time can be obtained.As mentioned abovecompared with the formerhigh-definition Still Picture Sub-Division can be picturized.[0068]By the wayalthough the area of the pixel is restrictedwhen the number of transistors is increased rapidlyaccording to itthe area of the photo-diode will decrease to it. Thenthe charge quantity Q generated with a photo-diode will decreaseand the sensitivity to a luminosity will become low as an image sensor. Howeverin the composition of this embodimentthe fall of the area of the above-mentioned photo-diode does not become disadvantageousbut works advantageously rather.
[0069]That isin this embodimentsince it can be expressed

with **V=Q/Cpxlchange **V of the potential of the terminal T1 can make an electric charge transfer factor highif Cpxl is made small. Thereforesensitivity will become fixed if only the rate to which the area of the photo-diode became small makes Cpxl small. The more it makes capacity Cpxl smallsince sensitivity becomes highthe more it becomes advantageous.
[0070]On the other handsince a kTC noise will become large in the conventional composition shown in drawing 8 or drawing 9 if capacity Cpxl is made small as shown in (3) types and (4) typesin the formerCpxl cannot be made small. Howeversince field shutter operation and removal of a kTC noise will be simultaneously attained if it has composition of this embodimentCpxl can be made small and area of a photo-diode can also be made small. Thereforeit is composition advantageous to a miniaturization.
[0071]Nexta 2nd embodiment of this invention is described. The feature of this invention is in the composition which makes the photo-diode which performs photoelectric conversionthe site which holds temporarily the carrier which the photo-diode generatedand the site which transforms the electric charge of a carrier into voltage become independentrespectively. Herenot a capacitor but an option is possible for the composition of the site which holds a carrier temporarily. Thenthis 2nd embodiment holds a carrier by a MOS gate.
[0072]Drawing 2 shows the representative circuit schematic for 1 pixel of a 2nd embodiment of the solid state camera which becomes this invention.Identical codes are given to drawing 1 and an identical configuration portion among the figure.According to this 2nd embodimentinstead of the capacitor Cex of drawing 1as shown in drawing 2the transistors M5 and M6 are approachedthe gate Mccd of MOS is arrangedand the feature is at the point using 2 d of pixels of the structure where an electric charge can be held under MOS gate Mccd.The potential at this time and the situation of movement of an electric charge are shown in drawing 3. Like drawing 1since Ce is the additional capacities for adjustmentomitting is a function.[0073]Nextoperation of this embodiment is explained with drawing 2 and drawing 3. 2 d of pixels presuppose that it is a pixel of a sequence with the line of somewhere middle which are not the top line of a solid state cameraand a lowermost row. It begins from the place said [that the output of the last signal of 2d of this pixel has just finished as a starting point of motion cycle explanationand].[0074]In this statethe transistor M1 and M6 are off and the terminal T1 is in the

state where it floated electrically. In the last cyclephoto-diode PD carried out photoelectric conversion to the terminal T1and the transistor M5Mccdand the electric charge transmitted through M6 remain in it as it is.The transistor M3 also serves as OFF and there is no output from 2d of this pixel to a column signal line. On the other handthe transistor M5 also serves as OFFand photo-diode PD performs photoelectric conversion like drawing 3 (A) in the state where it dissociated from others electricallyand is accumulating the electric charge like drawing 3 (B). Mccd also serves as OFFand it is in the state where an electric charge is not storedand it is in a state without an electric charge.[0075]In such the state2 d of pixels are waiting for CDS circuit 5 to end the processing which is a pixel of other lines. The one [the transistor M5 and MOS gate Mccd(s) / all the pixels including 2 d of pixels] like drawing 3 (C) all at once if signal read-out from all the pixels is completed and predetermined time passes since a photoelectric conversion start. Thenthe electric charge Q accumulated in photo-diode PD is simultaneously transmitted in the direction [directly under] of each MOS gate Mccd through each transistor M5 by all the pixels. As a resultthe electric charge of photo-diode PD is lost and is reset.

[0076]As shown in drawing 3 (D) after an end of charge transferthe transistor M5 is set to OFF and all electric charges are transmitted directly under MOS gate Mccd. Againphotoelectric conversion of photo-diode PD is carried outand it starts accumulation of an electric charge. On the other handMccd has become with one and continues holding an electric charge under a gate. 2 d of pixels are in such a stateand while CDS circuit 5 is processing a pixel of other linesthey continue standing by.

[0077]Thenif processing of 2 d of pixels currently observed starts2 d of pixels will perform a reset action of the terminal T1. That isa high-level signal from a control circuit which is not illustrated is impressed to a gate electrode of the transistor M1and makes M1 one. At this timethe transistor M3 and M6 are still OFF. As a resultpotential of the terminal T1 serves as (Vdd-Vthrst). HereVdd is power supply voltage and Vthrst is the threshold voltage of the transistor M1.

[0078]Thena signal to a gate electrode of the transistor M1 serves as a low leveland is made off [M1]. Therebythe terminal T1 returns to the state where it floated electricallyand a reset action completes it. Since the kTC noise ingredient Vktc rides on the terminal T1 at this

timepotential of the terminal T1 serves as (Vdd-Vthrst+Vktc).

[0079]On the other handpreparations for carrying out signal processing of 2 d of pixels even in CDS circuit 5 are made. That isthe switch S1 and S2 are closed and the terminal C2a and C1b are made into the reference potential Vref. Since M3 is considered as one by impressing a high-level signal from a control circuit which is not illustrated to a gate electrode of the transistor M3 in this statepotential of (Vdd-Vthrst+Vktc-Vthamp) is outputted to multiple-message-transmission item output linei.e.terminalC2b. HereVthamp is the threshold voltage of the transistor M2 for amplification. As a resultpotential difference of (Vdd-Vthrst+Vktc-Vthamp-Vref) is built over the capacitor C2.

[0080]NextCDS circuit 5 opens the switch S2sets it to OFFand changes the terminal C2a (= the terminal C1b) into the state where it floated. Hereby impressing a signal with the transistor M6 high-level from a control circuit which is not illustrated to the gate electrodeas shown in drawing 3 (E)M6 is considered as one.On the other handif a signal of a low level is impressed to MOS gate Mccdthe electric charge Q which was directly under Mccd will be transmitted to the terminal T1 through the transistor M6. The transistor M6 after charge transfer completion is set to OFFand as shown in drawing 3 (F)all the electric charges are transmitted to the terminal T1.

[0081]As a resultfor the terminal T1the electrical change by the electric charge Q is generated.Although the capacity Cpxl of the terminal T1 consists of the capacity of the capacitor Cegate capacitance Camp of the transistor M2and the diffusion capacitance Crst of the transistor M1 and the stray capacitance Cf of wiringwhen the electric charge Q enters herethe electrical change of **V=Q/Cpxl occurs.Thereforethe potential of the terminal T1 is set to (Vdd-Vthrst+Vktc+**V).

[0082]If an electrical change happens to the terminal T1it will be amplified by the source follower circuit with the transistor M2and also will be told through the transistor M3 in an ON state to multiple-message-transmission item output linei.e.terminalC2b.Therebythe potential of terminal C2b is set to (Vdd-Vthrst+Vktc-Vthamp+**V). That isthe electrical change produced in terminal C2b is (Vdd-Vthrst+Vktc-Vthamp+**V)-(Vdd-Vthrst+Vktc-Vthamp)=**VIt is influenced only by the ingredient by the charge quantity Q by the photoelectric conversion of photo-diode PDbut there is also no influence of a kTC noise.

[0083]According to the electrical change of this terminal

C2bthe electrical change of proportionality part Vref+ {**V-C1/(C1+C2)} with which the capacitor C1 and C2 were connected in series produces the terminal C2a (= terminal C1b) which is in the state which floated electrically.Thenthe switch S1 is openedit supposes that it is offand the processing result which is the above-mentioned electrical change is held to the capacitor C1. And it is supposed that the transistor M3 is off and the output from the pixel 2c is lost.[0084]Thenthe switch S3 is considered as one with the horizontal shift register which is not illustratedand the processing result of 2 d of pixels currently held at the capacitor C1 is outputted as a pixel signal through the switch S3.Thenthe switch S3 is opened againit is supposed that it is offand one cycle in 2 d of this pixel is completed. In the backthe same thing is again repeated from the beginning.[0085]Explanation of operation of the above-mentioned embodiment is an exampleand is not limited to this.For examplewhat is necessary is to perform reset with the transistor M1 of the terminal T1 by the above-mentioned explanationjust before outputting the reset potential of the terminal T1but just to perform it once to [somewhere in] the next signal output operationafter it is not limited to this and the last signal output finishes.[0086]Since the signal and background noise which carry out a total are taken by the above operation with the reset potential performed to the same timinga kTC noise is canceled. Since the electric charge all the pixel identical time carried out [the electric charge] photoelectric conversion is outputted from a horizontal shift register one by onea field shutter function is realized.[0087]Nextthe 3rd embodiment and 4th embodiment of this invention are described. The representative circuit schematic of the stroke matter of a 3rd embodiment of the solid state camera with which drawing 4 becomes this inventionand drawing 5 show the representative circuit schematic of the stroke matter of a 4th embodiment of the solid state camera which becomes this invention.Identical codes are given to drawing 1drawing 2and an identical configuration portion among both figuresand the explanation is omitted.[0088]According to 1st and 2nd old embodimentsreset of photo-diode PD was performed by the act of transmitting a carrier (electric charge). Howeverin this methodreset of photo-diode PD will be the exposure time which is 1 time and was always fixed to the 1 field. Since shutter speed cannot be freed nowit is convenient if the transistor for photo-diode reset which became independent to photo-diode PD is attached.

[0089]Soin a 3rd embodiment of this invention shown in drawing 4. The transistor M7 for photo-diode reset is formed in the pixel of a 1st embodimentand the transistor M7 for photo-diode reset is formed in the pixel of a 2nd embodiment in a 4th embodiment of this invention shown in drawing 5. That isin drawing 4 and drawing 5the N type layer of photo-diode PD is connected to the power supply voltage Vdd via the source of MOS type field effect transistor M7and the drain.[0090]Therebyin drawing 4 and drawing 5if a high-level reset signal is impressed to the gate of the transistor M7the transistor M7 is turned onand via the drain of the transistor M7and a sourcethe power supply voltage Vdd will be impressed to the N type layer of photo-diode PDand will reset this. That iseven if the carrier of photo-diode PD does not finish being transmittedphoto-diode PD is resettable to arbitrary timing by one [the transistor M7 / arbitrary timing].Thereforein 3rd and 4th embodimentsshutter time can be set up freely.[0091]In a 4th embodiment of drawing 5since the carrier holding portion is constituted from CCD type MOS gate Mccdthe potential of the portion in which the carrier directly under MOS gate Mccd is held with the potential of MOS gate Mccd can be moved freely. Therebyadvantageous operational mode can be set up.

[0092]Nextother operational modes of a 4th embodiment of this invention are explained.As a method of opening a dynamic rangethe method of adding what has short shutter timeand a long thing is known from before. It is 10msec which has long shutter timefor exampleand short things are for example0.5msec.

[0093]As everyone knowswhen shutter time is longa dark place is reflected wellbut a bright place will be poor white. On the other handwhen shutter time is shortalthough projection of a bright place becomes goodit will be black with a dark poor place. Thereforeif both information is addeda dark place and a bright place can be copied together.

[0094]Hereafteroperation in other modes of this 4th embodiment is concretely explained based on the composition shown in drawing 6 (A).Identical codes are given to drawing 5 and an identical configuration portion among the figure (A).The graphic display of the transistor M7M1 - M3 is omitted.Firstafter resetting photo-diode PDphotoelectric conversion between time Tl with longer shutter time is performed. thenthe potential of the channel of MOS gate Mccd applies the 1st potential that becomes in a potential minute half [about] when the potential of Vdd is applied to the gate electrode of Mccd to the gate electrode of Mccd.

[0095]If one [this state / the transistor M5]as shown in drawing 6 (B)a carrier (electric charge) will be transmitted under MOS gate Mccd through the transistor M5. Thenthe transistor M5 is made off.Therebyas shown in drawing 6 (B)the potential potential of the transistor M5 becomes highand an electric charge is held directly under MOS gate Mccd.[0096]Nextafter resetting photo-diode PD againonly Ts with short shutter time performs photoelectric conversion. As a black dot shows to drawing 6 (C) typicallyan electric charge is accumulated in photo-diode PD by this photoelectric conversion. Thenthe 2nd larger potentialfor exampleVddthan the 1st potential is impressed to the gate electrode of MOS gate Mccd. Therebythe potential potential directly under Mccd becomes still deeper than the last state.[0097]In this stateif the transistor M5 is oneas shown in drawing 6 (D)The electric charge accumulated in photo-diode PD flows into MOS gate Mccd through the transistor M5and the electric charge of this shutter time Ts is added to the electric charge at the time of the last shutter time Tl directly under Mccd. Thusif the made electric charge is outputted to Tlthe signal with which the dynamic range spread can be outputted.
[0098]Although NMOS FET is used in old explanationif N type and P type are replaced and the direction of voltage is made reverseof courseeffect same also at PMOS FET is acquired.
[0099]
[Effect of the Invention]As explained aboveafter accumulating the electric charge acquired by carrying out photoelectric conversion simultaneously with the photo-diode of all the pixels in charge storage partssuch as a capacitor and a MOS gateaccording to this inventionAfter facing outputting to the exterior through an output meansoperating the transistor for resetand an output means and sending out prescribed potential to a noise cancellerBy outputting the signal corresponding to the electric charge accumulated in the charge storage part to a noise canceller through an output meansHaving taken out only the signal component proportional to the electric charge produced by the photoelectric conversion of the photo-diode in the noise canceller A sakeField shutter operation by all the pixel simultaneous photoelectric conversion and removal (kTC noise removal) of the background noise in a noise canceller can be performed simultaneouslyandtherebyhigh-definition Still Picture Sub-Division can be picturized.
[0100]To the electric charge which carried out photoelectric conversion with the photo-diode by the 1st

shutter time of the longer one according to this invention. Since the electric charge which carried out photoelectric conversion with the photo-diode by the 2nd shutter time of the shorter one was added directly under the MOS gatethe signal with which the dynamic range spread can be outputted.
[0101]Since according to this invention the voltage in inverse proportion to the capacity in the common connection terminal of the transistor for resetthe 2nd transistor for charge transferand an output means constitutes so that it may produce for this common connection terminalSince the above-mentioned capacity is small made corresponding to making area of a photo-diode smallit can have composition advantageous to a miniaturization.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a representative circuit schematic for the stroke matter of a 1st embodiment of this invention.
[Drawing 2]It is a representative circuit schematic for the stroke matter of a 2nd embodiment of this invention.
[Drawing 3]It is a figure showing the potential of the important section of drawing 2and the situation of movement of an electric charge.
[Drawing 4]It is a representative circuit schematic of the stroke matter of a 3rd embodiment of this invention.
[Drawing 5]It is a representative circuit schematic of the stroke matter of a 4th embodiment of this invention.
[Drawing 6]It is a figure explaining operation in other modes of a 4th embodiment of this invention.
[Drawing 7]It is a block diagram of an example of the whole solid state camera.
[Drawing 8]It is a representative circuit schematic for the stroke matter of an example of the conventional solid state camera.
[Drawing 9]It is a representative circuit schematic for the stroke matter of other examples of the conventional solid state camera.
[Drawing 10]It is a figure showing making potential of a certain capacity C into a certain potential V.
[Explanations of letters or numerals]
1 Vertical shift register
2c and 2d Pixel of a 1st and 2nd embodiment
3 Load and a noise canceller
4 Horizontal shift register
5 CDS circuit

6 Load
PD Photo-diode
M1 Field effect transistor for reset
M2 Field effect transistor for amplification (output means)
M3 Field effect transistor for an output (output means)
M5 and M6 Transistor for charge transfer (the 1st2nd transistor for charge transfer)
M7 Field effect transistor for photo-diode reset
Mccd MOS gate
Cex Capacitor for charge storages
Ce Capacitor for capacity adjustments of a converter
S1S2and S3 Switch
T1 Terminal